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EXAMINER

KIM, JAY C

ART UNIT

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2815

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PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/743,793	Applicant(s) TANAHASHI ET AL.	
	Examiner JAY C. KIM	Art Unit 2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 30 December 2008.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,4-12 and 39 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,4-12 and 39 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 24 December 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

This Office Action is in response to the RCE filed December 30, 2008.

Claim Objections

1. Claims 1 and 39 are objected to because of the following informalities:

In claim 1, "SFQR" should be replaced by "Site Front least sQuare Range (SFQR)" on line 4, and "(atoms/cm³)or higher" should be replaced by "(atoms/cm³) or higher", and "semiconductor" should be inserted after "entire" on line 13.

On line 2 of claim 39, "CZ" should be replaced by "a Czochralski (CZ)".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claim 11 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention. Applicants originally disclosed in Fig. 15 of current Application that an oxide layer 35 is formed on a silicon substrate 34 that would become a crystal layer 36. Here, an SOI substrate is a composite layer of 31 and 35 formed by a bonding method. However, Applicants did not originally disclose that the oxide layer

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35 would contain carbon at a concentration recited in claim 1, since amended claim 1 recites a carbon concentration “throughout the entire substrate”.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 1, 4, 12 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujikawa (US 6,277,501) in view of Wenski et al. (US 6,458,688) and further in view of Asayama et al. (US 6,365,461).

Regarding claims 1 and 4, Fujikawa discloses a semiconductor substrate (Fig. 4, 5 or 6) comprising a front face and a rear face that are both mirror-polished (col. 9, lines 11-13, and col. 13, lines 46-56), wherein the semiconductor substrate contains boron (col. 12, lines 14-19), a crystal layer having a thickness of 3 μm is provided on the front face (col. 12, lines 61-65), and the semiconductor substrate contains carbon at a concentration of 1×10^{15} (atoms/cm³) or higher throughout the entire semiconductor substrate (col. 13, lines 35-39).

Fujikawa differs from the claimed invention by not showing that the semiconductor substrate meets an SFQR value ≤ 70 (nm) as a flatness of the front face, and contains boron at a concentration higher than or equal to 5×10^{16} (atoms/cm³) and lower than or equal to 2×10^{17} (atoms/cm³), wherein a minimum value of the

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concentration of boron [B] (atoms/cm³) is defined for a required thickness t (μm) of the crystal layer within the range of the concentration of boron, based on a relational equation $[B] \geq (2.2 \pm 0.2) \times 10^{16} \exp(0.21t)$ (claim 1), wherein a maximum value of a thickness t (μm) of the crystal layer is defined for a required concentration of boron [B] (atoms/cm³), based on a relational equation $[B] \geq (2.2 \pm 0.2) \times 10^{16} \exp(0.21t)$ (claim 4).

Wenski et al. disclose a semiconductor substrate (Fig. 1) comprising a front face and a rear face that are both mirror-polished (col. 7, lines 42-43), wherein the semiconductor substrate (Fig. 1) meets an SFQR value ≤ 70 (nm) or 0.07 μm (Please note that the numbers in Fig. 1 are in μm, because a maximum SFQR value is less than or equal to 0.13 μm (lines 3-5 of ABSTRACT).) as a flatness of the front face.

Since both Fujikawa and Wenski et al. teach a semiconductor substrate, it would have been obvious to the one of ordinary skill in the art at the time the invention was made that the semiconductor substrate disclosed by Fujikawa may comprise an SFQR value disclosed by Wenski et al., because a semiconductor substrate with a low SFQR value is suitable for fabricating semiconductor devices comprising small line widths and improving yield of the semiconductor devices.

Fujikawa in view of Wenski et al. differ from the claimed invention by not showing that the semiconductor substrate contains boron at a concentration higher than or equal to 5×10^{16} (atoms/cm³) and lower than or equal to 2×10^{17} (atoms/cm³), wherein a minimum value of the concentration of boron [B] (atoms/cm³) is defined for a required thickness t (μm) of the crystal layer within the range of the concentration of boron, based on a relational equation $[B] \geq (2.2 \pm 0.2) \times 10^{16} \exp(0.21t)$ (claim 1), wherein a

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maximum value of a thickness t (μm) of the crystal layer is defined for a required concentration of boron $[B]$ (atoms/cm^3), based on a relational equation $[B] \geq (2.2 \pm 0.2) \times 10^{16} \exp(0.21t)$ (claim 4).

Asayama et al. disclose a semiconductor substrate (col. 9, lines 43-45) containing boron at a concentration of 1×10^{17} (atoms/cm^3).

Since both Fujikawa and Asayama et al. teach a semiconductor substrate containing boron, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the semiconductor substrate disclosed by Fujikawa in view of Wenski et al. with the boron concentration disclosed by Asayama et al., because a boron concentration may be controlled to improve gettering efficiency of a semiconductor substrate. In this case, $[B] = 1 \times 10^{17} (\text{atoms}/\text{cm}^3) \geq (2.2 \pm 0.2) \times 10^{16} \exp(0.21 \times 3)$ in Fujikawa in view of Wenski et al. and further in view of Asayama et al. Further, the claims are prima facie obvious without showing that the claimed ranges of required thickness and boron concentration achieve unexpected results relative to the prior art range. *In re Woodruff*, 16 USPQ2d 1935, 1937 (Fed. Cir. 1990). See also *In re Huang*, 40 USPQ2d 1685, 1688 (Fed. Cir. 1996) (claimed ranges of a result effective variable, which do not overlap the prior art ranges, are unpatentable unless they produce a new and unexpected result which is different in kind and not merely in degree from the results of the prior art). See also *In re Boesch*, 205 USPQ 215 (CCPA) (discovery of optimum value of result effective variable in known process is ordinarily within skill of art) and *In re Aller*, 105 USPQ 233 (CCPA 1955) (selection of optimum ranges within prior art general conditions is obvious).

Regarding claim 12, Fujikawa in view of Wenski et al. and further in view of Asayama et al. disclose the semiconductor substrate according to claim 1.

The claim limitation “the rear face is in an exposed state, or a natural oxide film having a thickness of 1 (nm) or less is formed on the rear face” specifies an intended use or field of use, because, for example, if the semiconductor substrate is kept in vacuum, no natural oxide film would be formed on the rear face, and is treated as non-limiting since it has been held that in device claims, intended use must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. *In re Casey*, 152 USPQ 235 (CCPA 1967); *In re Otto*, 136 USPQ 458, 459 (CCPA 1963). A claim containing a “recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus” if the prior art apparatus teaches all the structural limitations of the claim. *Ex Parte Masham*, 2 USPQ 2d 1647 (Bd. Pat. App. & Inter. 1987).

Regarding claim 39, Fujikawa further disclose for the semiconductor substrate of claim 1 that the semiconductor substrate is a Czochralski (CZ) substrate (col. 9, lines 7-9).

6. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fujikawa (US 6,277,501) in view of Wenski et al. (US 6,458,688) and further in view of Asayama et al. (US 6,365,461) as applied to claim 1 above, and further in view of Takizawa et al.

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(US 5,734,195). The teachings of Fujikawa in view of Wenski et al. and further in view of Asayama et al. are discussed above.

Fujikawa in view of Wenski et al. and further in view of Asayama et al. differ from the claimed invention by not showing that the crystal layer is a silicon crystal layer formed by epitaxial growth.

Takizawa et al. disclose a semiconductor substrate (composite layer of 11 and 15 in Fig. 3C) (col. 4, lines 22-23 and 41), wherein a crystal layer (16) (col. 4, line 47) is provided on a front face (12), wherein the crystal layer (16) is a silicon crystal layer formed by epitaxial growth.

Since both Fujikawa and Takizawa et al. teach a semiconductor substrate, it would have been obvious to the one of ordinary skill in the art at the time the invention was made that the crystal layer disclosed by Fujikawa in view of Wenski et al. and further in view of Asayama et al. may be a silicon crystal layer formed by epitaxial growth, because forming an epitaxial silicon layer on a silicon wafer substrate is well-known to form a high quality silicon layer for a semiconductor device fabrication.

7. Claims 6-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujikawa (US 6,277,501) in view of Wenski et al. (US 6,458,688) and further in view of Asayama et al. (US 6,365,461) as applied to claim 1 above, and then further in view of Fitzgerald (US 2002/0123167). The teachings of Fujikawa in view of Wenski et al. and further in view of Asayama et al. are discussed above.

Regarding claim 6, Fujikawa in view of Wenski et al. and further in view of Asayama et al. differ from the claimed invention by not showing that the crystal layer is a silicon-germanium alloy crystal layer.

Fitzgerald discloses a semiconductor substrate (102 in Fig. 1), wherein a silicon-germanium alloy crystal layer (composite layer of 104 and 106) is provided on a front face.

Since both Fujikawa and Fitzgerald teach a semiconductor substrate, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the semiconductor substrate disclosed by Fujikawa in view of Wenski et al. and further in view of Asayama et al. with the silicon-germanium alloy crystal layer disclosed by Fitzgerald, because forming a silicon-germanium alloy crystal layer on a silicon substrate is well-known in manufacturing a semiconductor device to apply strain on a channel layer that will be formed on the silicon-germanium alloy crystal layer.

Regarding claim 7, Fujikawa in view of Wenski et al. and further in view of Asayama et al. differ from the claimed invention by not showing that the crystal layer is a layer in a layered structure of a silicon-germanium alloy crystal layer and a silicon crystal layer.

Fitzgerald discloses a semiconductor substrate (504 in Fig. 5D) (lines 5-9 of [0035]), wherein a layered structure (composite layer of 502 and 508) (line 17 of [0035]) of a silicon-germanium alloy crystal layer (502) and a silicon crystal layer (508) is provided on a front face of the substrate (504).

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Since both Fujikawa and Fitzgerald teach a semiconductor substrate, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the semiconductor substrate disclosed by Fujikawa in view of Wenski et al. and further in view of Asayama et al. with the layered structure of a silicon-germanium alloy crystal layer and a silicon crystal layer disclosed by Fitzgerald, because forming a layered structure of a silicon-germanium alloy crystal layer and a silicon crystal layer on a silicon substrate is well-known in manufacturing a semiconductor device to apply strain on the silicon layer that will be used as a channel layer.

Regarding claims 7 and 8, Fujikawa in view of Wenski et al. and further in view of Asayama et al. differ from the claimed invention by not showing that the crystal layer is a layer in a layered structure of a silicon-germanium alloy crystal layer and a silicon crystal layer (claim 7), wherein the silicon crystal layer is formed in an SOI structure in which the silicon crystal layer is separated by a silicon oxide layer (claim 8).

Fitzgerald discloses a layered structure (composite layer of 800, 802 and 808 in Fig. 8B) (lines 1-2 and 6-7 of [0041]) of a silicon-germanium alloy crystal layer (800) and two silicon crystal layers (802 and 808), wherein the top silicon poly-crystal layer (808) is formed in an SOI structure in which the top silicon poly-crystal layer (808) is separated by a silicon oxide layer (806).

Since both Fujikawa and Fitzgerald teach a semiconductor substrate, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the semiconductor substrate disclosed by Fujikawa in view of Wenski

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et al. and further in view of Asayama et al. with the layered structure of a silicon-germanium alloy crystal layer and two silicon crystal layers separated by a silicon oxide layer disclosed by Fitzgerald, because the top silicon poly-crystal layer and the silicon oxide layer would protect the strained silicon layer during semiconductor processing.

8. Claims 9-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujikawa (US 6,277,501) in view of Wenski et al. (US 6,458,688) and further in view of Asayama et al. (US 6,365,461) as applied to claim 1 above, and further modified by Inazuki et al. (US 6,362,076). The teachings of Fujikawa in view of Wenski et al. and further in view of Asayama et al. are discussed above.

Regarding claims 9 and 11, Fujikawa in view of Wenski et al. and further in view of Asayama et al. differ from the claimed invention by not showing that the semiconductor substrate is an SOI substrate, and wherein the crystal layer is an upper silicon crystal layer separated by a silicon oxide layer (claim 9), wherein the SOI substrate is formed by a bonding method (claim 11).

Inazuki et al. disclose a semiconductor substrate (6 in Fig. 1), which is an SOI substrate (col. 4, lines 48-50 and 52-53, and col. 5, line 6), and a crystal layer (7) (col. 5, lines 6-7) separated from the SOI substrate (6) by a silicon oxide layer (3) (col. 4, line 54), wherein the SOI substrate (6) is formed by a bonding method.

Since both Fujikawa and Inazuki et al. teach a semiconductor substrate, it would have been obvious to the one of ordinary skill in the art at the time the invention was made to combine the semiconductor substrate disclosed by Fujikawa in view of Wenski et al. and further in view of Asayama et al. with the wafer bonding method disclosed by

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Inazuki et al., because the resulting structure can be used for forming a field effect transistor using the SOI channel layer to improve semiconductor device performance.

Regarding claim 10, Fujikawa in view of Wenski et al. and further in view of Asayama et al. disclose the semiconductor substrate according to claim 9.

The limitation that “the SOI substrate is formed by a SIMOX method” is a product-by-process limitation that does not structurally distinguish the claimed invention over the prior art. Note that a product by process claim is directed to the product per se, no matter how actually made, *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See also *In re Brown*, 173 USPQ 685; *In re Luck*, 177 USPQ 523; *In re Fessmann*, 180 USPQ 324; *In re Avery*, 186 USPQ 161; *In re Wertheim*, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and *In re Marosi et al*, 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a product by process claim, and not the patentability of the process, and that an old or obvious product by a new method is not patentable as a product, whether claimed in product by process claims or not. Note that applicant has the burden of proof in such cases, as the above case law makes clear.

Response to Arguments

9. Applicants' arguments with respect to claim 1 have been considered but are moot in view of the new ground of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAY C. KIM whose telephone number is (571)270-1620. The examiner can normally be reached on 7:30 AM - 5:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on (571) 272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/J. K./
Examiner, Art Unit 2815
March 10, 2009

/Jerome Jackson Jr./
Primary Examiner, Art Unit 2815